Ku-band Super Low-noise Pseudomorphic Heterojunction Field-effect Transistors (HJFET) with High Producibility and High Reliability

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Abstract

This paper reports newly developed Ku-band super low-noise pseudomorphic heterojunction FETs (HJFET) with high producibility and high reliability, utilizing a novel electron beam lithography technique. The developed HJFETs with 0.25μm long and 200μm wide gate FETs showed average noise figure of 0.6 dB with 11.3 dB average associated gain at 12GHz, and exhibited high reliable operation with MTTF (mean time to failure) of $3x10^9$ hours at 100°C.

Introduction

In accordance with increasing demand for further noise reduction in front-end receivers for direct broadcasting satellite and communication systems, the development of super low-noise FETs has been actively pursued [1],[2]. Recently, to make further improvement in noise performance, InGaAs/AlGaAs pseudomorphic FETs has been mainly developed instead of the conventional AlGaAs/GaAs systems [3]-[7].

In this paper we report on newly developed super low-noise heterojunction FETs (HJFET) with modulation doped and pseudomorphic epilayer structures. The developed 0.25μm T-shaped gate HJFETs with 200μm gate width for Ku-band applications exhibit typical noise figure (NF) of 0.6 dB with 11.3 dB typical associated gain (Ga) at 12 GHz, and exhibit high reliable operation with MTTF (mean time to failure) of $3x10^9$ hours at 100°C.

Device Structure and Fabrication Process

Devices were fabricated on InGaAs/AlGaAs heterostructure layers grown by molecular beam epitaxy (MBE). The layer structure consists of a $3x10^{18}$ cm^{-3} Si-doped GaAs layer, a $2x10^{18}$ cm^{-3} Si-doped AlGaAs layer, an un-doped InGaAs channel layer, and an un-doped GaAs buffer layer. The thickness of the InGaAs channel layer is 150 A, and the InAs mole fraction is 0.15.

The measured sheet carrier concentration (Ns) and the electron Hall mobility (μ) of the epitaxial wafers for the developed HJFETs fabrication are $2x10^{12}$ cm^{-2} and 5800 $cm^2V^{-1}s^{-1}$ at 300 K and $1.8x10^{12}$ cm^{-2} and 18000 $cm^2V^{-1}s^{-1}$ at 77 K, respectively.

The developed HJFETs were fabricated with 0.25μm gate length and 200μm total gate width. The distance between source and drain contacts is 3.0μm. For high frequency low-noise applications, low gate resistance and short gate length are indispensable. For this purpose, novel direct-write electron-beam lithography technique with a PMMA(I)/PMMA(II) (HI/LOW) double layer system is employed for Ti-Al T-shaped gate formation [8]. The device employs a recessed gate structure and a gate Schottky contact is formed on the n-AlGaAs layer. Fig.1 shows a cross sectional view of the fabricated HJFET.

Except for the gate fabrication step, the device fabrication process is simple. The first step was a mesa formation by wet etching. Next ohmic contacts were defined by evaporation, lift-off and alloying. After the gate fabrication step described above, the silicon-nitride films were deposited. The final step in device fabrication was a formation of Ti-Pt layers followed by Au plating for the bonding pads.

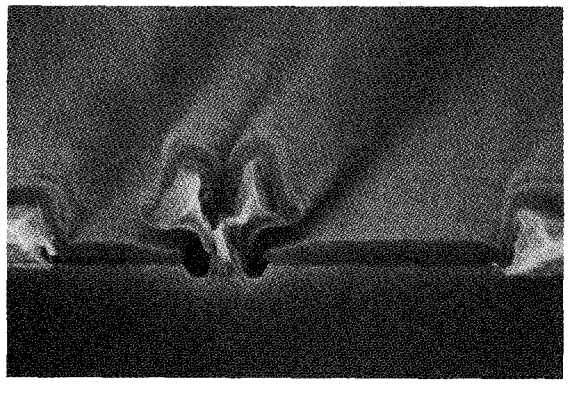

Fig.1 Cross sectional view of a developed HJFET.

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DC and RF Performance

The developed pseudomorphic HJFETs exhibit excellent DC and microwave performances.

Fig.2 shows a typical drain I-V characteristics and Table.1 summarizes the measured typical device characteristics. The maximum extrinsic transconductances (Gmmax) are 410-470 mS/mm, and the extrinsic transconductances (Gm) are 300-330 mS/mm at operation bias point(V_{DS}=2V, I_{DS}=10mA). The source access resistance and gate parasitic resistance are about 2.2Ω and 0.9Ω, respectively.

Microwave performance has been measured at 12GHz in the packaged form. Fig.3 shows the distributions of noise figure and associated gain. The number of samples was 700 from 35 wafers. Average noise figure and its standard deviation at V_{DS}=2V and I_{DS}=10mA are 0.6 dB and 0.03 dB with an average associated gain of 11.3 dB and a 0.3 dB standard deviation, respectively. Scattering in S-parameters is also very small. These results show an excellent uniformity of the device characteristics for the developed HJFETs.

The dependence of noise figure and associated gain on the drain current is shown in Fig.4. As seen from Fig.4, the noise figure is very insensitive to drain current. The noise figure is less than 0.7dB in the drain current range from 6 to 30mA.

In addition to low noise figure and high gain performances, the observed bias dependence shows an advantage of the developed pseudomorophic HJFETs over the conventional FETs based on AlGaAs/GaAs heterojunction structures, and is very attractive for practical applications in microwave amplifiers.

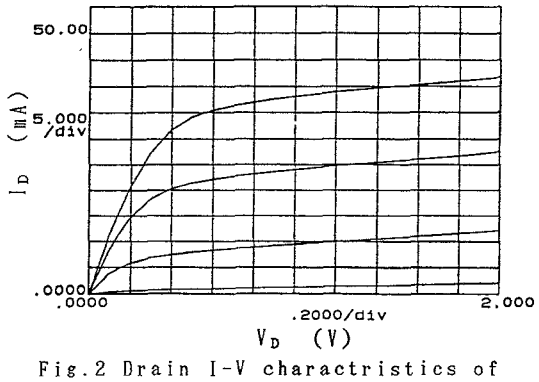

Fig.2 Drain I-V charactristics of a 200μm gate width HJFET. (H:0.2V/div, V:5mA/div, Gate: -0.2V/step)

Item	Gmmax	Gm	Rs	Rg
Typ.	88mS	62mS	2.2Ω	0.9Ω
Item	Cgs	Cgd	NF	Ga
Typ.	0.18pF	0.03pF	0.6dB	11.3dB

Table.1 Typical device charactristics.

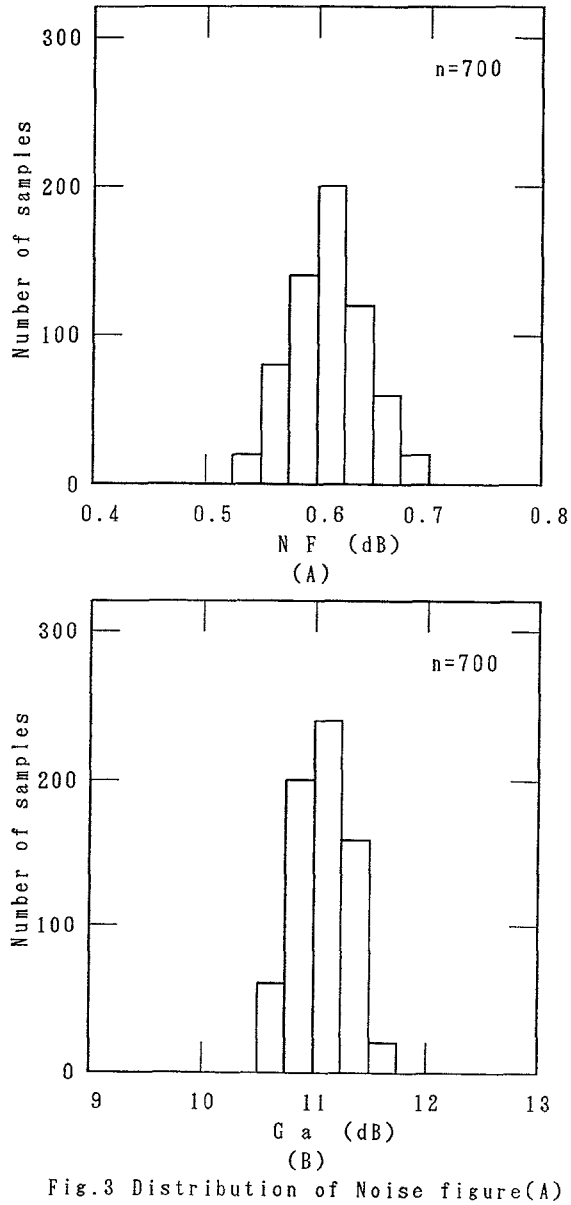

Fig.3 Distribution of Noise figure(A) and associated gain(B). (V_{DS}=2V, I_{DS}=10mA, f=12GHz)

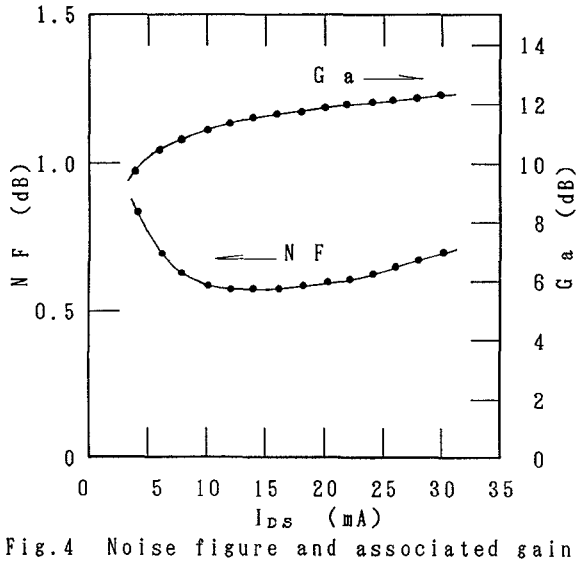

Fig.4 Noise figure and associated gain as a function of drain current. (V_{DS}=2V, f=12GHz)

Reliability Qualification

The reliability qualification tests were carried out for the newly developed pseudomorophic HJFET. The test results show superior reliability.

The reliability tests consists of following items;

a) High temperature DC bias test
b) High temperature reverse bias test
c) High temperature storage test
d) γ-ray irradiation test

Fig.5 shows the results of high temperature DC bias tests. Fig.6 shows the results of high temperature reverse bias tests. Any degradation of microwave performance was not observed up to 3000 hours as shown in Fig.5 and Fig.6.

In order to investigate metallurgical stability, high temperature storage tests at 259°C, 295°C and 337°C were performed. From the test results, no degradiation was observed except for Schottky barrier gate degradation caused by the variation of Schottky barrier height. But this variation is not considered to influence the life time at practical device operation temperature. These high temperature storage test gave an MTTF (mean time to failure) of arroud 3×10^9 hours at Tch=100°C with activation energy of 1.67 eV.

Radiation hardness was also evaluated for the HJFETs using Co-60 γ-ray, resulting in no degradiation of device charactristics up to the dose of 1×10^7 rad.

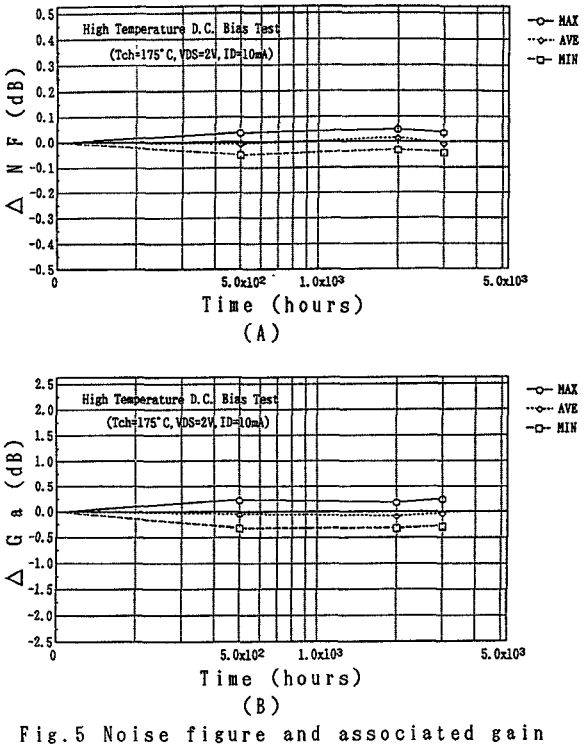

Fig.5 Noise figure and associated gain as a function of test time. (High temperature DC bias test, at Tch=175°C, V_{DS}=2V, I_{DS}=10mA) (A) ΔNF, (B) ΔGa

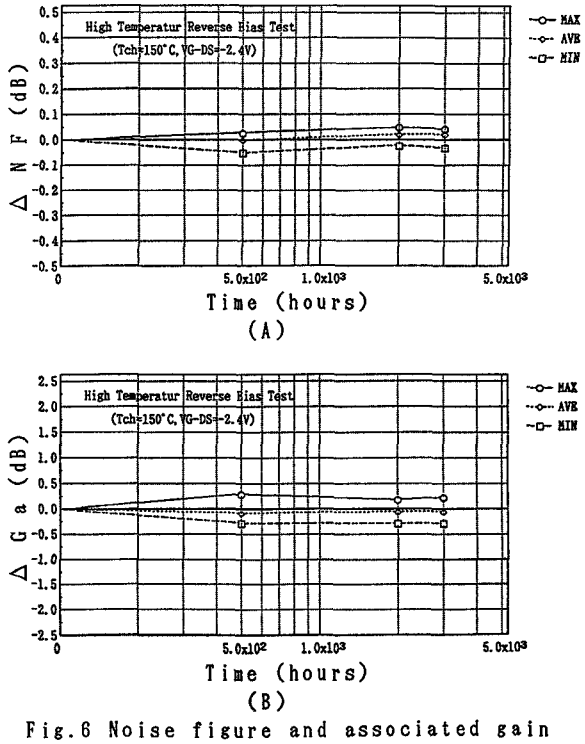

Fig.6 Noise figure and associated gain as a function of test time. (High temperature reverse bias test, at Tch=150°C, V_{G-DS}=-2.4V) (A) ΔNF, (B) ΔGa

Conculusion

A new super low-noise HJFET with pseudomorphic epilayer structure has been developed. The developed 0.25μm T-shaped gate HJFET with 200μm gate width showed average noise figure of 0.6dB with 11.3dB associated gain at 12GHz, and exhibited high reliable operation with MTTF of 3×10^9 hours at Tch=100°C.

From these good microwave characteristics and high reliability results, the developed HJFETs are promising for Ku-band applications as an alternative to conventional AlGaAs/GaAs HJFETs.

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